Amendments to the Claims:
This listing of claims will replace all prior versions and listings, of claims in the present application.

Listing of Claims:

Claims 1- 11 cancelled

Claim 12 (original) A method for forming a field effect transistor comprising the steps of:

a) providing a conductive substrate; then

b) etching said substrate to form an upstanding pillar adjacent a substantially-planar upper surface of said etched substrate; then

c) forming a stack of substantially-planar layers of material adjacent said pillar, said stack of material comprising a first insulator layer adjacent said upper surface of said etched substrate, a gate layer of conductive material overlying said first insulator layer and a second insulator layer overlying said gate layer; then

d) etching said pillar to the level of said substantially-planar upper surface of said etched substrate to form a upstanding pore within said stack; then

e) forming a gate insulator layer at the interior of said upstanding pore; then

f) forming an upstanding channel of semiconductor material having a top region and a bottom region interior of said gate insulator layer; and then

g) heavily doping said top region of said upstanding channel of semiconductor material.

Claim 13 (original) A method as defined in Claim 12 wherein the step of etching said substrate further includes the steps of:

a) masking said substrate with a nanoparticle; and then

b) directionally etching said masked substrate whereby whereby said pillar is a nanopillar and said pore is a nanopore.

Claim 14 (original) A method as defined in Claim 13 further including the step of depositing a layer of conductive material in contact with said gate layer at the interior of said nanopore.

Claim 15 (original) A method as defined in Claim 13 further characterized in that the step of forming an upstanding channel of semiconductor material further includes the step of epitaxially growing said channel from said substrate.

Claim 16 (original) A method as defined in Claim 15 wherein said substrate comprises single crystal silicon.

Claim 17 (original). A method as defined in Claim 13 wherein said substrate comprises a highly-doped semiconductor material.

Claim 18 (original) A method as defined in Claim 17 wherein said substrate comprises highly-doped silicon.

Claim 19 (original) A method as defined in Claim 12 wherein said gate layer comprises a metal.

Claim 20 (original) A method as defined in Claim 12 wherein said gate layer comprises a highly-doped semiconductor.

Claim 21 (original) A method for forming a field effect transistor comprising the steps of:

a) providing a substrate of semiconductor material; then

b) etching said substrate to form an upstanding pillar adjacent a substantially-planar upper surface of said etched substrate; then

c) creating a conductively-doped region within said etched substrate substantially and immediately beneath said pillar; then

d) forming a stack of substantially-planar layers of material adjacent said pillar, said stack of materials comprising a first insulator layer adjacent said upper surface of said etched substrate, a gate layer of conductive material overlying said first insulator layer and a second insulator layer overlying said gate layer; then

e) etching said pillar to the level of said substantially-planar upper surface of said etched substrate to form an upstanding pore within said stack; then

f) forming a gate insulator layer interior to said upstanding pore; then

g) forming an upstanding channel of semiconductor material having a top region and a bottom region interior of said gate insulator layer; and then

h) heavily doping said top region of said upstanding channel.

Claim 22 (original) A method as defined in Claim 21 wherein the step of etching said substrate further includes the steps of:

a) masking said substrate with a nanoparticle; and then

b) directionally etching said masked substrate whereby whereby said pillar is a nanopillar and said pore is a nanopore.

Claim 23 (original) A method as defined in Claim 22 further including the step of depositing a layer of conductive material in contact with said gate layer at the interior of said nanopore.

Claim 24 (original) A method as defined in Claim 22 further characterized in that the step of forming an upstanding channel of semiconductor material further includes the step of epitaxially growing said channel from said substrate.

Claim 25 (original) A method as defined in Claim 24 wherein said substrate comprises single crystal silicon.

Claim 26 (original) A method as defined in Claim 21 wherein said gate layer comprises a metal.

Claim 27 (original) A method as defined in Claim 21 wherein said gate layer comprises a highly-doped semiconductor.

Claim 28 (original) A method for forming a field effect transistor comprising the steps of:

a) providing a substrate having an upper surface; then

b) forming a stack of substantially-planar layers of material on said substrate, said stack comprising a first insulator layer adjacent said upper surface of said substrate, a gate layer of conductive material overlying said first insulator layer and a second insulator layer overlying said gate layer; then

c) forming an overlayer on top of said second insulator layer; then

d) masking said overlayer with a nanoparticle; then

e) directionally etching said overlayer to form an upstanding nanopillar on top of said second insulator layer; then

f) depositing a second overlayer on top of said second insulator layer and said upstanding nanopillar; then

g) removing said second overlayer to the top of said upstanding nanopillar; then

h) removing said nanopillar to leave an upper nanopore within said second overlayer defining an etch mask; then

i) directionally etching a lower nanopore to said upper surface of said substrate; then

j) removing said second overlayer; then

k) forming a gate insulator layer at the interior of said upstanding nanopore; then

l) forming an upstanding channel of semiconductor material having a top region and a bottom region interior of said gate insulator layer; and then

m) heavily doping said top region of said upstanding channel of semiconductor material.

Claim 29 (original) A method as defined in Claim 28 further including the step of depositing a layer of conductive material in contact with said gate layer at the interior of said nanopore.

Claim 30 (original) A method as defined in Claim 28 further characterized in that the step of forming an upstanding channel of semiconductor material further includes the step of epitaxially growing said channel from said substrate.

Claim 31 (original) A method as defined in Claim 30 wherein said substrate comprises single crystal silicon.

Claim 32 (original) A method as defined in Claim 28 wherein said gate layer comprises a metal.

Claim 33 (original) A method as defined in Claim 28 wherein said gate layer comprises a highly-doped semiconductor.